UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,898	12/21/2001	Yuji Yoshimoto	217502US2	5325

22850 7590 09/10/2004

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
HARTMAN JR, RONALD D	

ART UNIT	PAPER NUMBER
2121	

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,898	YOSHIMOTO ET AL.	
	Examiner	Art Unit	
	Ronald D Hartman Jr.	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,9,10,16,17,22,25,28-30,32,34,36,38 and 40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,9,10,16,17,22,25,28-30,32,34,36,38 and 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims:

1. 3-8, 11-15, 18-21, 23-24, 26-27, 31, 33, 35, 37, 39 and 41-43 are canceled; and
2. 1-2, 9-10, 16-17, 22, 25, 28-30, 32, 34, 36, 38 and 40 are currently pending.

Response to Arguments

3. Applicant's arguments with respect to the pending claims, listed above, have been considered but are moot in view of the new ground(s) of rejection, as set forth below in this office action.

Priority

4. Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Claim Objections

5. Claims 30, 32, 34 and 36 are objected to because they refer to "a detection means" and the examiner cannot specifically find, within the specification, what is actually meant by the "detection means". Therefore this feature has been interpreted to be equivalent to any mechanism by which "the quantity of information is detected" in a memory or other data storage device.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 9, 16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seaton et al., U.S. Patent No. 5,591,299, in view of Jensen et al., U.S. Patent No. 5,555,195.

As per claims 1, 9 and 16, Seaton et al. teaches a processing apparatus (Examiners Note: "apparatus" is interpreted as per Merriam Webster's Collegiate Dictionary; Tenth Edition; "*a set of* materials or *equipment* designed *for a particular use*."; i.e. a system), the apparatus comprising:

- an apparatus body for executing a prescribed process to a target object (i.e. Figure 1B element 10; "Spray Processor");
- a control mechanism for controlling the apparatus body (i.e. "controller"; Figure 1B element 12);
- an information storage section (i.e. Figure 1B, element 103 or Figure 1B, element 26 or Figure 1B, elements 109a or 109b.) for receiving signals communicated to and from the control mechanism (i.e. C4 L51-56), the signals containing information necessary for grasping an operational record of the processing apparatus body during real time execution of the prescribed process to the target object (i.e. Abstract, claim 1 and Figures 3-16), and
- wherein the information includes alarm data notifying malfunctions and troubles in said processing apparatus body during the execution of the prescribed process (i.e. Figures 6-7 and 9) .

As per claims 1, 9 and 16, Seaton et al. does not specifically teach information being stored every 2 seconds.

Jensen et al. teaches a controller for use in an environment control network that stores diagnostic information (title) and Jensen further teaches that during operation, a processor periodically samples sensors to develop averages of parameter values and to provide diagnostic information over the lifetime of the controller, wherein the run time information is sampled and stored every 1.5 seconds (i.e. C6 L21-30 and C6 L58-L67).

Although Jensen does not specifically teach 2 seconds, the choice of 2 seconds over any other amount of time, in this instance 1.5 seconds, appears to simply be a design choice. In the examiners opinion, so long as the information is collected in a timely fashion, that is, in a way that allows for adequate descriptions of the process to be gathered, or archived, the actual choice for the time would depend on the complexities of the system and or the needs or desires of an operator, and therefore using 2 seconds instead of 1.5 seconds, as taught by Jensen, or using 5 seconds instead of 2 seconds, as another example, would depend on the system, and since this specific time choice of 2 seconds does not appear to provide the claimed invention any specific advantage or novelty, its inclusion is believed to be an obvious variation of the archiving taught by Seaton. However, in the interest in showing an actual teaching of archiving data every "specific amount of time", the Jensen et al reference has been applied.

Therefore, for at least the aforementioned reasons, the inclusion of Jensen et al. into Seaton et al. would have been obvious since data relating to the process obviously needs to be stored and or refreshed in a manner that allows for an accurate representation of the process under control, that is, in a timely fashion, as already discussed, and since this is most easily accomplished through implementation of a feature whereby information is stored at time intervals, that way the data can be later reviewed if need be, and this would have been obvious to one of ordinary skill in the art at the time the invention was made.

As per claim 22, Seaton et al teaches lots (i.e. Abstract, "lot scheduling").

8. Claims 2, 10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seaton's combined system (Seaton in view of Jensen), as applied to claims 1, 9 and 16 above, in further view of Goder et al., U.S. Patent No. 6,424,880.

As per claims 2, 10 and 17, Seaton et al. does not specifically teach a semiconductor processing apparatus which utilizes two controllers since Seaton's

disclosure is directed towards using a single processing chamber in conjunction with a single controller.

Goder et al. teaches a semiconductor processing apparatus that utilizes more than one chamber and more than one controller (i.e. Figure 4 elements 406, 408, 414 and 416 for two controllers, one for each chamber A and B, and two processors, one for each chamber A and B).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated the teachings of Goder et al into the system disclosed by Seaton et al. for the purpose of allowing the semiconductor processing apparatus the ability to react quickly to changing parameters so as to maintain rapidly changing desired conditions of a wafer within a wafer processing chamber while utilizing more than one processing chamber concurrently, and this would have been obvious to one of ordinary skill in the art at the time the invention was made.

9. Claims 25 and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seaton et al., U.S. Patent No. 5,591,299, in view of Goder et al., U.S. Patent No. 6,424,880.

As per claim 25, Seaton et al. teaches a processing apparatus (Examiners Note: "apparatus" is interpreted as per Merriam Webster's Collegiate Dictionary; Tenth Edition; "*a set of* materials or *equipment* designed *for a particular use*."; i.e. a system), the apparatus comprising:

- an apparatus body for executing a prescribed process to a target object (i.e. Figure 1B element 10; "Spray Processor");
- a control mechanism for controlling the apparatus body (i.e. "controller"; Figure 1B element 12);
- an data storage section (i.e. Figure 1B, element 103 or Figure 1B, element 26 or Figure 1B element 109b.) for receiving signals communicated to and from the control mechanism (i.e. C4 L51-56), the signals containing information necessary for grasping an operational record of the processing apparatus body during real time execution of

the prescribed process to the target object (i.e. Abstract, claim 1 and Figures 3-16),

- wherein the information includes alarm data notifying malfunctions and troubles in said processing apparatus body during the execution of the prescribed process (i.e. Figures 6-7 and 9) and that data is stored every prescribed period (i.e. at the end of each process run, C5 L33-46);
- an information process section for receiving the information from the apparatus body and analyzing the information (i.e. Figure 1B element 102); and
- a monitor computer connected through a communication network with the information process section for receiving the information (i.e. Figure 1B element 102 or 109a).

As per claim 25, Seaton et al. does not specifically teach a semiconductor processing apparatus which utilizes two controllers since Seaton's disclosure is directed towards using a single processing chamber in conjunction with a single controller.

Goder et al. teaches a semiconductor processing apparatus that utilizes more than one chamber (i.e. apparatus bodies) and more than one controller (i.e. Figure 4 elements 406, 408, 414 and 416 for two controllers, one for each chamber A and B, and two processors, one for each chamber A and B).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated the teachings of Goder et al into the system disclosed by Seaton et al. for the purpose of allowing the semiconductor processing apparatus the ability to react quickly to changing parameters so as to maintain rapidly changing desired conditions of a wafer within a wafer processing chamber while utilizing more than one processing chamber concurrently, and this would have been obvious to one of ordinary skill in the art at the time the invention was made.

As per claim 28, Seaton teaches the use of a display for displaying alarm information (i.e. Figure 6).

As per claim 29, Seaton et al teaches the control mechanism (i.e. "controller") having a display (i.e. Figure 1B element 26).

10. Claims 30, 32, 34, 36, 38 and 40 are rejected as being unpatentable over Seaton et al., as applied to claims 1, 9 and 16 above, in view of Bims et al., U.S. Patent Application No. 2002/0019965.

As per claims 30, 32, 34, 36, 38 and 40, Seaton does not specifically teach memory management techniques wherein information may be deleted to make room for new incoming data.

Bims et al. teaches a memory within a device that processes information about incoming data and when a determination is made that the amount of space available is less than needed, oldest data is deleted or erased, to make room for the new data (i.e. [0038]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the teachings of Bims et al into the system of Seaton for the purpose of allowing for efficient memory management so data is not lost when a memory, which has certain size limitations, is running out of available space, and this would have been obvious to one of ordinary skill in the art at the time the invention was made.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ronald D Hartman Jr. whose telephone number is 703-308-7001. The examiner can normally be reached on Mon. - Fri., 11:30 am - 8:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on 703-308-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ronald D Hartman Jr.
Examiner
Art Unit 2121

Anthony Knight
Supervisory Patent Examiner
Group 3600